ISEDA 2025

2025 International Symposium of EDA

May 9-12, 2025 | Hong Kong Disneyland, China

CALL FOR PAPERS

Scope

Sponsored by IEEE and ACM, and jointly organized by EDA^2 and the EDA Committee of CIE, the ISEDA (International Symposium of EDA) is an annual premier forum dedicated to VLSI design automation. The symposium aims at exploring the new challenges, presenting leading-edge technologies and providing EDA community with opportunities of predicting future directions in EDA research areas. ISEDA covers the full range of EDA topics from device and circuit levels up to system level, from analog to digital designs as well as manufacturing. The format of meeting intends to cultivate productive and novel interchangeable ideas among EDA researcher and developers. Academic and industrial EDA related professionals who are interested in EDA's theoretical and practical research are all welcomed to contribute to ISEDA.

Advisors

IEEE/CEDA, ACM/SIGDA

Department of Information Science, National Natural Science Foundation of China (NSFC)

Chinese Institute of Electronics (CIE)

Steering Committee, Major Plan of "Fundamental Research on Post-Moore Novel Devices"

Organizers

EDA Ecosystem Development Accelerator (EDA^2)

EDA Committee of CIE

Co-Organizers

The Chinese University of Hong Kong

Peking University

Southeast University

Tsinghua University

Xidian University

Committee

Executive Committee

General Chairs

- **Ru Huang,** President of Southeast University, Academician of the Chinese Academy of Sciences
- **Yue Hao,** Professor of Xidian University, Academician of the Chinese Academy of Sciences

Steering Committee

- **Shaojun Wei,** Tsinghua University
- **Xuan Zeng,** Fudan University
- **Patrick Girard,** French National Center for Scientific Research
- **Jamal Deen,** McMaster University
- **Yankin Tanurhan,** Synopsys

Technical Program Committee

Conference Chairs

- **Tsung-Yi Ho,** The Chinese University of Hong Kong
- **Runsheng Wang,** Peking University
- **Gang Qu,** University of Maryland

Technical Program Chairs

- **Bei Yu,** The Chinese University of Hong Kong
- **Yun Liang,** Peking University
- **Ulf Schlichtmann,** Technical University of Munich

Special Session Chair

- **Wenjian Yu,** Tsinghua University

Industrial Session Chair

- **Fan Yang,** Shenzhen GWX Technology Co.,Ltd.

Tutorial/Training Chair

- **Zuochang Ye,** Tsinghua University

Finance Chair

- **Gang Chen,** Nanjing Industrial Innovation Center of EDA

Panel Chair

- **Yibo Lin,** Peking University

Publication Chair

- **Qiang Xu,** The Chinese University of Hong Kong

Industry Liaison

- **Yutao Ma,** Primarius Technologies Co.,Ltd

Publicity Chair

- **Xin Li,** Duke Kunshan University

Outreach Chairs

- **[US] Hai Zhou,** Northwestern University
- **[Canada] Peter Chun,** University of Alberta
- **[Europe] Zebo Peng,** Linköping University
- **[Asia] Xiaoqing Wen,** Kyushu Institute of Technology

Track Committee

System-Level Modeling and Design Methodology
Chair: Jieru Zhao, Shanghai Jiao Tong University
Co-Chair: Qi Sun, Zhejiang University

Memory Architecture and Near/In Memory Computing
Chair: Xiaoming Chen, Institute of Computing Technology, CAS
Co-Chair: Li Du, Nanjing University

Analog-Mixed Signal Design Automation
Chair: Fan Yang, Fudan University
Co-Chair: Keren Zhu, Fudan University

High-Level, Behavioral, and Logic Synthesis and Optimization
Chair: Zhufei Chu, Ningbo University
Co-Chair: Weikang Qian, Shanghai Jiao Tong University

Analysis and Optimization for Power and Timing
Chair: Yibo Lin, Peking University
Co-Chair: Zhiyao Xie, HKUST

Physical Implementation
Chair: Hailong Yao, University of Science and Technology Beijing
Co-Chair: Yuzhe Ma, HKUST (GZ)

Testing, Validation, Simulation, and Verification
Chair: Huawei Li, Institute of Computing Technology, CAS
Co-Chair: Hongce Zhang, HKUST (GZ)

Design for Manufacturability and Reliability
Chair: Lan Chen, Institute of Microelectronics, CAS
Co-Chair: Yu-Guang Chen, National Central University

Packaging & Multi-Physics Simulation
Chair: Hongliang Lu, Xidian University
Co-Chair: Yarui Peng, University of Arkansas

Technology & Modeling
Chair: Lining Zhang, Peking University
Co-Chair: Hao Yan, Southeast University

Emerging Technologies and Applications
Chair: Xiangshui Miao, HUST
Co-Chair: Hailong You, Xidian University

AI & Open Source EDA
Chair: Guojie Luo, Peking University
Co-Chair: Xingquan Li , Peng Cheng Laboratory

Areas of Interest

Original papers in, but not limited to, the following areas are invited.

- [1] System-Level Modeling and Design Methodology:
  - 1.1 HW/SW co-design, co-simulation and co-verification
  - 1.2 System-level design exploration, synthesis, and optimization
  - 1.3 System-level formal verification
  - 1.4 System-level modeling, simulation and validation
  - 1.5 Networks-on-chip and NoC-based system design
  - 1.6 Constructing hardware in scala embedded language
- [2] Memory Architecture and Near/In Memory Computing:
  - 2.1 Storage system and memory architecture
  - 2.2 On-chip memory architectures and management: Scratchpads, compiler controlled memories, etc.
  - 2.3 Memory/storage hierarchies and management for emerging memory technologies
  - 2.4 Near-memory and in-memory computing
- [3] Analog-Mixed Signal Design Automation:
  - 3.1 Analog/mixed-signal/RF synthesis
  - 3.2 Analog layout, verification, and simulation techniques
  - 3.3 High-frequency electromagnetic simulation of circuit
  - 3.4 Mixed-signal design consideration
- [4] High-Level, Behavioral, and Logic Synthesis and Optimization:
  - 4.1 Digital simulation / emulation
  - 4.2 High-Level synthesis
  - 4.3 Logic synthesis
  - 4.4 Synthesis for approximate computing
- [5] Analysis and Optimization for Power and Timing:
  - 5.1 Deterministic/statistical timing analysis and optimization
  - 5.2 Process technology modeling for timing analysis
  - 5.3 Power modeling, analysis and simulation
  - 5.4 Low-power design and optimization at circuit and system levels
  - 5.5 Thermal aware design and dynamic thermal management
  - 5.6 Energy harvesting and battery management
- [6] Physical Implementation:
  - 6.1 Floorplanning, partitioning, placement and routing optimization
  - 6.2 Interconnect planning and synthesis
  - 6.3 Clock network synthesis
  - 6.4 Physical design of 3D/2.5D IC and package (e.g., TSV, interposer, monolithic)
  - 6.5 Post layout and post-silicon optimization
  - 6.6 Layout verification
- [7] Testing, Validation, Simulation, and Verification:
  - 7.1 RTL and gate-leveling modeling, simulation, and verification
  - 7.2 Circuit-level formal verification
  - 7.3 ATPG, BIST and DFT
  - 7.4 System test and 3D IC test, online test and fault tolerance
  - 7.5 Memory test and repair
- [8] Design for Manufacturability and Reliability:
  - 8.1 Design-technology co-optimization (DTCO)
  - 8.2 Standard and custom cell design and optimization
  - 8.3 Reticle enhancement, lithography-related design optimizations and design rule checking
  - 8.4 Design for manufacturability, yield, defect tolerance, cost issues, and DFM impact
  - 8.5 Device-, gate, and circuit-level techniques for reliability analysis and optimization (e.g., soft error, aging, etc.)
  - 8.6 Post-Layout optimizations
- [9] Packaging & Multi-Physics Simulation:
  - 9.1 Extraction, TSV, and package modeling
  - 9.2 Chiplet design and design tools
  - 9.3 Chip level thermal simulation
  - 9.4 Packaging stress analysis
  - 9.5 Multi-physics simulation
  - 9.6 Signal/power integrity, EM modeling and analysis
- [10] Technology & Modeling:
  - 10.1 Device compact modeling
  - 10.2 Process design Kit
  - 10.3 Semiconductor process & device simulation
  - 10.4 Cell library design, characterization and verification
  - 10.5 New transistor/device and process technology: spintronic, phase-change, single-electron, 2D materials, etc.
- [11] Emerging Technologies and Applications:
  - 11.1 Biomedical, biochip, nanotechnology, MEMS
  - 11.2 Design automation for 3D ICs and heterogeneous integration
  - 11.3 Design automation for quantum computing
  - 11.4 Design automation for silicon photonics
  - 11.5 Design automation for compound semiconductors verification
- [12] AI & Open Source EDA:
  - 12.1 Artificial Intelligence for EDA
  - 12.2 Cloud / Parallel Computing for EDA
  - 12.3 Open Source EDA
  - 12.4 EDA database
  - 12.5 EDA standardization

Submission

Invited Talks: Need an abstract **within one page**.

Extended Abstract: **1-2 pages**.

Regular Paper: **4-6 pages**.

Follow the standard double column template:

https://www.ieee.org/conferences/publishing/templates.html

Will select **best paper award, best student paper, best Ph.D. dissertation award** after the presentations.

Submission system is available soon.

Scan the QR code above or copy the link to enter the submission system.

https://www.eda2.com/conferenceHome/submissionHome

Important Dates

Deadline for Regular Paper Submission: **February 10, 2025**

Notification of Acceptance: **March 10, 2025**

Deadline for Final Version: **March 31, 2025**

Deadline for Invited Talks, Extended Abstracts, Tutorials, Special Sessions, Industry Sessions: **March 15, 2025**

Liaison

IEEE/CEDA Representative: Tsung-Yi Ho

CIE Representative: Shouyi Yin

Website Chair: Huixin Tang

Secretary: Xiakai Wang

Contact

Contact: Yu Huang **Email**: huangyu61@hisilicon.com

Conference Secretary: Joyce Zhong **Email**: iseda@eda2.com **Tel:** +86-186 2826 3876

https://www.eda2.com/iseda/index.html