ISEDA 2025 Agenda Overview

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May 9-12, 2025								
09:00-18:00	Sign-in & Conference Materials Collection							
May 9, 2025 | Friday								
12:00:-14:00	*Lunch*							
14:00-17:00	Tutorial 1	Test and Health Monitoring under Approximations and Variations	Hans-Joachim Wunderlich					
	Tutorial 2	Advanced Open-Source FPGA HLS and Physical Implementation Tools	Zhi-Xiong Di, Zhe Lin, Jiarui Wang, Jing Mai					
	Tutorial 3	VLSI Physical Design, From 2D to 3D	Hailong Yao, Yuanqing Cheng, Hao Yan					
	Tutorial 4	AHS: An EDA toolbox for Agile Chip Front-end Design	Yun Liang, Jingwen Leng					
	Tutorial 5	Formal Verification for EDA	Shaowei Cai, Hongce Zhang					
	Tutorial 6	LLM Application in EDA	Bei Yu, Ying Wang, Ansuman Banerjee					
	Tutorial 7	AI-Driven Breakthroughs in Next-Generation Circuit Simulation and Reliability	Zhou Jin, Zhenya Zhou, Dan Niu					
May 10, 2025| Saturday								
08:30-09:00	Opening Ceremony							
09:00-09:40	Keynote Speech 1	Prof. Giovanni De Micheli, École polytechnique fédérale de Lausanne (EPFL) *The Future of Computing Systems Design*						
09:40-10:20	Keynote Speech 2	Prof. Jaijeet Roychowdhury, University of California, Berkeley *Oscillator Ising Machines: Principles and Design*						
10:20-10:40	Break		*Speaker(s) & Paper ID(s)*					
10:40-12:00	Technical Session 1	System-Level Simulation, Modeling, and Co-Verification	Zebo Peng *(Invited)*	60	122	154		
	Technical Session 2	Innovative Simulation and Data Compression for Verification	Sybille Hellebrand *(Invited)*	5	182	241		
	Technical Session 3	Emerging Transistor Technologies and Novel Process Innovations	119	135	137	151		
	Technical Session 4	Emerging Technologies and Applications in EDA	157	195	227	162		
	Technical Session 5	Large Language Models and Next-Generation EDA Tools	Han Yu *(Track Keynote)*	205	32			
12:00-14:00	Lunch & Keynote 3 & 4	Mr. Albert Wong, Hong Kong Science & Technology Parks Corporation *Title TBA*						
		Dr. Hong Zhou, Huawei *Title TBA*						

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May 10, 2025 | Saturday								
14:00-15:40	Technical Session 6	Analog/Mixed-Signal Synthesis and Layout Optimization	52	57	64	70	83	
	Technical Session 7	High-Level and Behavioral Synthesis: Trends and Optimization	98	129	136	143	145	
	Technical Session 8	Physical Design and 3D/2.5D Integration Techniques	Chen Wu *(Invited)*	192	193	203	219	
	Technical Session 9	Reliability Engineering and Post-Layout Optimization	Weiwei Pan *(Track Keynote)*	133	178	200	216	
	Technical Session 10	AI-Driven Design Automation and Open Source Initiatives	112	128	140	173	174	
	Special Session 1	CEDA-adjoint special session: Deep Learning Inspired Algorithms for Physical Modeling and Analysis of Advanced IC Design	Yibo Lin, Zhou Jin, Yuanqing Cheng, Wenjian Yu					
	Panel 1	Scaling up AI-Assisted EDA Techniques with Large Foundation AI Models	Qiang Xu, Cheng Zhuo, Fan Yang, Huawei Li, Yun Liang, Mingxuan Yuan					
15:40-16:00	Break							
15:40-16:00	Poster Session	Paper ID: 12, 16, 41, 45, 53, 54, 72, 76, 78, 87, 94, 104, 111, 144, 149, 153, 158, 160, 167, 169, 181, 191, 199, 204, 208, 215, 217, 220, 247	*Speaker(s) & Paper ID(s)*					
16:00-18:00	Technical Session 11	Innovations in Memory Architecture and Near/In-Memory Computing	97	110	156	224	238	239
	Technical Session 12	Advanced Floorplanning and Macro Placement	31	34	36	69	89	
	Technical Session 13	Design-Technology Co-Optimization and Manufacturability	Primarius *(Invited)*	22	198	231	232	194
	Technical Session 14	Efficient Parameter Extraction and Modeling Techniques	25	229	230	235	237	221
	Technical Session 15	Large Language Models and Next-Generation EDA Tools	Bing Li *(Invited)*	184	202	242	15	
	Special Session 2	Bridging AI and Hardware: Advancing Specialized Circuits, Design Automation, and Manufacturing	Kuncai Zhong, Zhiyao Xie, Zhenge Jia, Zheyu Yan					
	Panel 2	AI/LLM for IC Manufacturing	Lan Chen, Xiaoming Liu, Hao Geng, Mingxuan Yuan, Xingsheng Wang					
18:30	Gala Dinner							

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May 11, 2025 | Sunday								
09:00-09:40	Keynote Speech 5	Prof. Sung-Kyu Lim, Georgia Institute of Technology (Gatech) *Enhancing AI Chip Design: AI and Traditional Algorithms for Multi-Chip Integration*						
09:40-10:20	Keynote Speech 6	Prof. Ulf Schlichtmann, Technical University of Munich (TUM) *Optical Networks-on-Chip: EDA for the Future of Interconnect*						
10:20-10:40	Break		*Speaker(s) & Paper ID(s)*					
10:40-12:00	Technical Session 16	Power Modeling, Analysis, and Thermal Management	11	152	165	180		
	Technical Session 17	Advanced Test Methodologies and DFT Techniques	Hans-Joachim Wunderlich *(Invited)*	114	118	127		
	Technical Session 18	Device Compact Modeling and Process Simulation	Lan Wei *(Invited)*	40	95	132		
	Technical Session 19	Emerging Technologies and Applications in EDA	Heng Wu *(Invited)*	Pei-Hsin Ho *(Invited)*	17			
12:00-14:00	Lunch & Keynote 7 & 8	Prof. Georges Gielen, KU Leuven (University of Leuven) *DeepDesignAMS: Will Tomorrow's Analog Integrated Circuits be Generated by AI?*						
		Prof. Jinjun Xiong, University at Buffalo *Title TBA*						
14:00-15:40	Technical Session 20	Advanced Analog Simulation and Verification Techniques	91	176	183	223	226	
	Technical Session 21	Routing, Interconnect, and Partitioning Innovations	92	102	109	130	187	
	Technical Session 22	Artificial Intelligence in EDA: Library, Innovation and Applications	Xingquan Li *(Invited)*	9	35	43	63	
	Panel 3	The Fusion of AI and Multiphysics: Accelerating EDA Revolution	Zhou Jin, Qinzi Xu, Ting-Jung Lin, Xingsheng Wang, Pinghao Jia					
16:00	Social Event	Disneyland Park						

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May 12, 2025| Monday								
09:00-09:40	Keynote Speech 9	Prof. Tim Kwang-Ting CHENG, The Hong Kong University of Science and Technology *Design and EDA for Edge Inference Chips Supporting Large-Scale Multi-Modal AI Models: The InnoHK ACCESS Approach*						
09:40-10:20	Keynote Speech 10	Prof. Sachin Sapatnekar, University of Minnesota *Automating Analog Design for the 21st Century*						
10:20-10:40	Break		*Speaker(s) & Paper ID(s)*					
10:40-12:00	Technical Session 23	Advanced Timing Analysis and Optimization	59	81	179	42		
	Technical Session 24	System-Level Design Exploration and NoC Innovations	66	68	168	171		
	Technical Session 25	RTL and Gate-Level Simulation and Verification	51	142	170	212		
	Technical Session 26	Packaging, Chiplet Design, and Multi-Physics Simulation	21	55	96	126		
	Technical Session 27	Advanced Simulation and Optimization in Semiconductor Processes	175	196	210	211		
12:00-14:00	Lunch & Keynote 11	Assoc. Prof. Vijay Janapa Reddi, Harvard University *Architecture 2.0: Foundations of Artificial Intelligence Agents for Modern Computer System Design*						
14:00-	Departure							