

CALL FOR PAPERS

Scope

Advised by IEEE/CEDA and ACM/SIGDA, and organized by EDA², the ISEDA (International Symposium of EDA) is an annual premier forum dedicated to VLSI design automation. The symposium aims at exploring the new challenges, presenting leading-edge technologies and providing EDA community with opportunities of predicting future directions in EDA research areas. ISEDA covers the full range of EDA topics from device and circuit levels up to system level, from analog to digital designs as well as manufacturing. The format of meeting intends to cultivate productive and novel interchangeable ideas among EDA researcher and developers. Academic and industrial EDA related professionals who are interested in EDA's theoretical and practical research are all welcomed to contribute to ISEDA.

AdvisorsIEEE/CEDA
ACM/SIGDA**Organizer**EDA Ecosystem Development Accelerator (EDA²)**Co-organizers**Singapore Semiconductor Industry Association
Siliconexus Pte Ltd

Committee

Executive Committee**General Chairs**

- Prof. Hao, Yue, Xidian University, Academician of the Chinese Academy of Sciences
- Prof. Wang, Runsheng, Peking University

Steering Committee

- Prof. Wei, Shaojun, Tsinghua University
- Prof. Zeng, Xuan, Fudan University
- Dr. Girard, Patrick, French National Center for Scientific Research
- Prof. Deen, Jamal, McMaster University
- Dr. Tanurhan, Yankin, Synopsys

Technical Program Committee**Conference Chairs**

- Dr. Hui, Chiu Wing Colin, GlobalFoundries
- Prof. Ho, Tsung-Yi, The Chinese University of Hong Kong
- Prof. Qu, Gang, University of Maryland

Technical Program Chairs

- Prof. Yu, Bei, The Chinese University of Hong Kong
- Prof. Schlichtmann, Ulf, Technical University of Munich
- Ms. Leung, Kafai, A*STAR Institute of Microelectronics

Keynote Chair

- Prof. Liang, Yun, Peking University

Panel Chair

- Mr. Ong, Jonathan, Applied Materials

Industry Chair

- Mr. Lam, Lup Meng, Synopsys

Publicity Chair

- Prof. Basu, Kanad, Rensselaer Polytechnic Institute

Tutorial Chair

- Prof. Sasan, Avesta, University of California, Davis

Tutorial Co Chair

- Prof. Lim, Yeow Kheng, National University of Singapore

Special Session Chair

- Prof. Ghosh, Swaroop, The Pennsylvania State University

Outreach Chair US

- Prof. Forte, Domenic, University of Florida

Outreach Chair Europe

- Prof. Halak, Basel, University of Southampton

Outreach Chair Asia

- Prof. Li, Yongfu, Shanghai Jiao Tong University

Outreach Chair Canada

- Prof. Chun, Peter, University of Alberta

Track Committee**System-Level Modeling and Design Methodology**

- Chairs: Sun, Qi, Zhejiang University

Zhao, Jieru, Shanghai Jiao Tong University

Memory Architecture and Near/In Memory Computing

- Chairs: Chen, Xiaoming, Institute of Computing Technology, CAS

Zhang, Li, Technical University of Darmstadt

Analog-Mixed Signal Design Automation

- Chairs: Zhu, Keren, Fudan University

Du, Li, Nanjing University

High-Level, Behavioral, and Logic Synthesis and Optimization

- Chairs: Qian, Weikang, Shanghai Jiao Tong University

Pilato, Christian, Politecnico di Milano

Analysis and Optimization for Power and Timing

- Chairs: Xie, Zhiyao, The Hong Kong University of Science and

Technology

Li, Bing, Technische Universität Ilmenau

Physical Implementation

- Chairs: Ma, Yuzhe, The Hong Kong University of Science and

Technology (Guangzhou)

Lin, Yibo, Peking University

Testing, Validation, Simulation, and Verification

- Chairs: Zhang, Hongce, The Hong Kong University of Science and

Technology (Guangzhou)

Zheng, Yuanjin, Nanyang Technological University

Design for Manufacturability and Reliability

- Chairs: Chen, Yu-Guang, National Central University

Li, Meng, Peking University

Packaging & Multi-Physics Simulation

- Chairs: Peng, Yarui, Southeast University

Tseng, Tsun-Ming, Technical University of Munich

Technology and Modeling

- Chairs: Ng, Kian Ann, DigiPen Institute of Technology Singapore

Chen, Quan, Southern University of Science and Technology

Emerging Technologies and Applications

- Chairs: Lee, Vincent, National University of Singapore

Li, Xingquan, Peng Cheng Laboratory

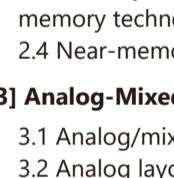
AI & Open Source EDA

- Chairs: Yu, Cunxi, University of Maryland

Tan, Chee Wei, Nanyang Technological University

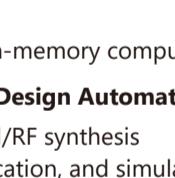
Keynote Speakers

More speakers will be updated soon.



Prof. Benini, Luca

Università di Bologna



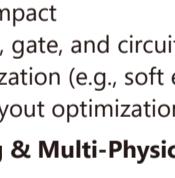
Prof. Yeo, Yee Chia

Deputy Chief Executive (Innovation & Enterprise) A*STAR



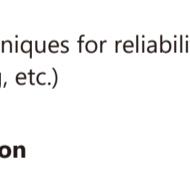
Mr. Kengeri, Subramani

Corporate Vice President and GM Systems to Materials (STM) Applied Materials



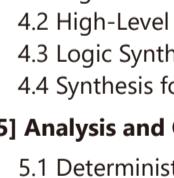
Prof. Yeo, Seng Kiat

Singapore University of Technology and Design



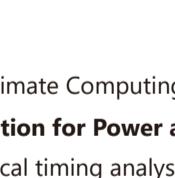
Mr. Chan, Don

Vice president, Research & Development Cadence Design Systems, Inc.



Prof. Parhi, Keshab

University of Minnesota



Prof. Chakrabarty, Krishnendu

Arizona State University



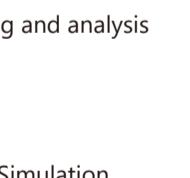
Prof. Alioto, Massimo

National University of Singapore



Prof. Takahashi, Atsushi

Institute of Science Tokyo



Prof. Wunderlich, Hans-Joachim

University of Stuttgart

Areas of Interest

Original papers in, but not limited to, the following areas are invited.

[1] System-Level Modeling and Design Methodology

- 1.1 HW/SW co-design, co-simulation and co-verification
- 1.2 System-level design exploration, synthesis, and optimization
- 1.3 System-level formal verification
- 1.4 System-level modeling, simulation and validation
- 1.5 Networks-on-chip and NoC-based system design
- 1.6 Constructing hardware in scala embedded language

[2] Memory Architecture and Near/In Memory Computing

- 2.1 Storage system and memory architecture
- 2.2 On-chip memory architectures and management: Scratchpads, compiler, controlled memories, etc.
- 2.3 Memory/storage hierarchies and management for emerging memory technologies
- 2.4 Near-memory and in-memory computing

[3] Analog-Mixed Signal Design Automation

- 3.1 Analog/mixed-signal/RF synthesis
- 3.2 Analog layout, verification, and simulation techniques
- 3.3 High-frequency electromagnetic simulation of circuit
- 3.4 Mixed-signal design consideration

[4] High-Level, Behavioral, and Logic Synthesis and Optimization

- 4.1 Digital Simulation / Emulation
- 4.2 High-Level Synthesis
- 4.3 Logic Synthesis
- 4.4 Synthesis for Approximate Computing

[5] Analysis and Optimization for Power and Timing

- 5.1 Deterministic/statistical timing analysis and optimization
- 5.2 Process technology modeling for timing analysis
- 5.3 Power modeling, analysis and simulation
- 5.4 Low-power design and optimization at circuit and system levels

- 5.5 Thermal aware design and dynamic thermal management
- 5.6 Energy harvesting and battery management

[6] Physical Implementation

- 6.1 Floorplanning, partitioning, placement and routing optimization
- 6.2 Interconnect planning and synthesis
- 6.3 Clock network synthesis
- 6.4 Physical design of 3D/2.5D IC and package (e. g., TSV, interposer, monolithic)
- 6.5 Post layout and post-silicon optimization
- 6.6 Layout verification

[7] Testing, Validation, Simulation, and Verification

- 7.1 RTL and gate-level modeling, simulation, and verification
- 7.2 Circuit-level formal verification
- 7.3 ATPG, BIST and DFT
- 7.4 System test and 3D IC test, online test and fault tolerance
- 7.5 Memory test and repair

[8] Design for Manufacturability and Reliability

- 8.1 Design-technology co-optimization (DTCO)
- 8.2 Standard and custom cell design and optimization
- 8.3 Reticle enhancement, lithography-related design optimizations and design rule checking
- 8.4 Design for manufacturability, yield, defect tolerance, cost issues, and DFM impact
- 8.5 Device-, gate, and circuit-level techniques for reliability analysis and optimization (e.g., soft error, aging, etc.)
- 8.6 Post-Layout optimizations

[9] Packaging & Multi-Physics Simulation

- 9.1 Extraction, TSV, and package modeling
- 9.2 Chiplet Design and Design tools
- 9.3 Chip Level Thermal Simulation
- 9.4 Packaging Stress Analysis

- 9.5 Multi-Physics Simulation
- 9.6 Signal/Power integrity, EM modeling and analysis

[10] Technology & Modeling

- 10.1 Device Compact Modeling
- 10.2 Process Design Kit
- 10.3 Semiconductor Process & Device Simulation
- 10.4 Library Design, Characterization and Verification
- 10.5 New transistor/device and process technology: spintronic, phase-change, single-electron, 2D materials, etc.

[11] Emerging Technologies and Applications

- 11.1 Biomedical, biochip, nanotechnology, MEMS
- 11.2 Design automation for 3D ICs and heterogeneous integration
- 11.3 Design automation for quantum computing
- 11.4 Design automation for silicon photonics
- 11.5 Design automation for compound semiconductors verification

[12] AI & Open Source EDA

- 12.1 Artificial Intelligence for EDA
- 12.2 Cloud / Parallel Computing for EDA
- 12.3 Open Source EDA
- 12.4 EDA Database
- 12.5 EDA Standardization

Submission

Invited Talks: Need an abstract **within one page**.Extended Abstract: **1-2 pages**.Regular Paper: **4-6 pages**.Please make sure there is **NO AUTHOR INFORMATION** in your submission, and you can download the paper template through the website: <https://www.eda2.com/iseda/sub.html>**Best Paper Award, Honorable Mention Paper Award** will be selected after the presentations.

Submission system is open now.

Scan the QR code or copy the following link to enter the submission system.

<https://www.eda2.com/conferenceHome/submitHome>