ISEDA 2024

2024 International Symposium of EDA
Hybrid Conference

May 10-13, 2024 | Xi'an, China

CALL FOR PAPERS

Scope

Jointly organized by EDA^2 and EDA Committee of CIE, the ISEDA (International Symposium of EDA) is an annual premier forum dedicated to VLSI design automation. The symposium aims at exploring the new challenges, presenting leading-edge technologies and providing EDA community with opportunities of predicting future directions in EDA research areas. ISEDA covers the full range of EDA topics from device and circuit levels up to system level, from analog to digital designs as well as manufacturing. The format of meeting intends to cultivate productive and novel interchangeable ideas among EDA researcher and developers. Academic and industrial EDA related professionals who are interested in EDA's theoretical and practical research are all welcomed to contribute to ISEDA.

Advisors

IEEE/CEDA, ACM/SIGDA

Department of Information Science, National Natural Science Foundation of China (NSFC)

Chinese Institute of Electronics (CIE)

Steering Committee, Major Plan of " Fundamental Research on Post-Moore Novel Devices"

Organizers

EDA Ecosystem Development Accelerator (EDA^2)

EDA Committee of CIE

Co-Organizers

Xidian University
Peking University
Southeast University
Tsinghua University

Committee

Executive Committee

General Chairs:

Ru Huang
President of Southeast University
Academician of the Chinese Academy of Sciences

Yue Hao
Professor of Xidian University
Academician of the Chinese Academy of Sciences

Steering Committee

Shaojun Wei
Xuan Zeng
Patrick Girard

Technical Program Committee

Conference Chairs:
Zhangming Zhu
Runsheng Wang
Jun Yang
Technical Program Chairs:
Hailong You
Yun Liang
Hao Yan
Special Session Chair: Wenjian Yu
Industrial Session Chair: Fan Yang
Tutorial/Training Chair: Zuochang Ye
Finance Chair: Gang Chen
Keynote Speaker Chair: Wanli Chang
Panel Chair: Yibo Lin
Local Arrangements Chair: Xiaoning He
Session Chair: Cheng Zhuo
Publication Chair: Qiang Xu
Industry Liaison: Yutao Ma
Exhibition Chair: Megy Wang
Publicity Chair : Xin Li
Outreach Chair – US: Hai Zhou
Outreach Chair – Canada: Peter Chun
Outreach Chair – Europe: Zebo Peng
Outreach Chair – Asia: Xiaoqing Wen

Track Committee

Technology & Model Chair: Xingsheng Wang
Technology & Model Co-Chair: Lining Zhang

Analog Circuit Chair: Fan Yang
Analog Circuit Co-Chair: Hao Yu

Packaging & Multi-Physics Chair: Hongliang Lu
Packaging & Multi-Physics Co-Chair: Min Tang

Wafer Manufacturing Chair: Lan Chen
Wafer Manufacturing Co-Chair: Yayi Wei

Digital Design & Verification Chair: Zhufei Chu
Digital Design & Verification Co-Chair: Yong Fu

Physical Implementation Chair: Hailong Yao
Physical Implementation Co-Chair: Peng Cao

Emerging Technology Chair: Bei Yu
Emerging Technology Co-Chair: Li Jiang

EDA foundation & Standards Chair: Xiaohui Tan
EDA foundation & Standards Co-Chair: Duanduan Jian

Open source EDA Track Chair: Huawei Li
Open source EDA Track Co-chair: Guojie Luo

EDA Contest Chair: Longxing Shi
EDA Contest Chair Co-Chair: Zhixiong Di

Areas of Interest

Original papers in, but not limited to, the following areas are invited.

- [1] Technology & Model:
  - 1.1 Device Compact Modeling
  - 1.2 Process Design Kit
  - 1.3 Semiconductor Process & Device Simulation
  - 1.4 Cell Library Design, Characterization and Verification
- [2] Analog Circuit:
  - 2.1 Schematic & Layout Design
  - 2.2 Circuit Simulation
  - 2.3 On-chip & Packaging Electromagnetic Field Simulation
  - 2.4 Radio-Frequency & Photoelectric Compound Circuit Simulation
- [3] Digital Design & Verification:
  - 3.1 Digital Simulation / Emulation
  - 3.2 High-Level Synthesis
  - 3.3 Logic Synthesis
  - 3.4 Formal Verification
  - 3.5 Constructing Hardware in Scala Embedded Language
- [4] Physical Implementation:
  - 4.1 Design-For-Test, Design-For-Reliability, Design-For-Manufacturability
  - 4.2 Placement & Routing
  - 4.3 Parasitic Extraction
  - 4.4 Timing Analysis
  - 4.5 Physical Verification
  - 4.6 Electromigration & IR drop
- [5] Wafer Manufacturing:
  - 5.1 Computational Lithography
  - 5.2 Masking Manufacturing
  - 5.3 Yield & Defect Analysis
  - 5.4 Process Modeling and Emulation
  - 5.5 Metrology and Silicon Data Processing
  - 5.6 APC (Automatic Process Control) Technology
- [6] Packaging & Multi-Physics:
  - 6.1 Packaging Design
  - 6.2 Chip Level Thermal Simulation
  - 6.3 Packaging Stress Analysis
  - 6.4 Multi-Physics Simulation
- [7] Emerging Technologies:
  - 7.1 Artificial Intelligence for EDA
  - 7.2 Cloud / Parallel Computing for EDA
  - 7.3 Heterogeneous Computing for EDA
- [8] Miscellaneous:
  - 8.1 Open Source EDA
  - 8.2 EDA Database
  - 8.3 EDA Standardization

Submission

Invited Talks: Need an abstract within one page.

Extended Abstract: 1-2 pages.

Regular Paper: 4-6 pages.

Follow the standard double column template:

https://www.ieee.org/conferences/publishing/templates.html

Will select best paper award, best student paper, best Ph.D. dissertation award after the presentations.

Submission System

Scan the QR code above or copy the link to enter the submission system.

https://www.eda2.com/conferenceHome/submissionHome

Important Dates

Deadline for Regular Paper Submission:
~~February 10, 2024~~
February 28, 2024(Extended)
Notification of Acceptance:
~~March 06, 2024~~
March 25, 2024(Extended)
Deadline for Final Version:
~~March 31, 2024~~
April 10, 2024(Extended)
Deadline for Invited Talks, Extended Abstracts, Tutorials, Special Sessions, Industry Sessions: March 15, 2024

Liaison

IEEE/CEDA Representative: Tsung-Yi Ho
CIE Representative: Shouyi Yin
Website Chair: Huixin Tang
Secretary: Xiakai Wang

Contact

Contact: Yu Huang **Email**: huangyu61@hisilicon.com

Conference Secretary: Joyce Zhong **Email**: iseda@eda2.com **Tel:** +86-186 2826 3876

https://www.eda2.com/iseda/index.html