ISEDA 2024 Conference Program Overview

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May 10-13, 2024		
10:00-18:00	**Sign-in & Conference Materials Collection**	
May 10, 2024 | Friday		
14:00-17:00	**Tutorial 01**	Test and Health Monitoring under Approximations and Variations
	Tutorial 02	Design Automation of Analog Circuits
	Tutorial 03	Agile Design Tools for In-Memory Computing Systems: from Macro Circuit to Architecture
	Tutorial 04	Boolean Satisfiability Solving, State-of-the-Art
	Tutorial 05	Benchmark for 2023 Integrated Circuit EDA Elite Challenge
	Tutorial 06	Enabling Large Language Models in EDA
	Tutorial 07	iEDA: An Open-source Physical Design EDA Infrastructure and Toolchain
	Tutorial 08	Introducing Building Blocks of DTCO
	Tutorial 09	Chip Verification Solution Based on Formal Verification
	Tutorial 10	Practical Training: Application of Chip Verification Solutions
	Tutorial 11	Training and Demonstration of EDA Tools for the Full Process of RF Circuit Design
	Tutorial 12	Design Enablement Solution for Novel Semiconductor Devices Research
18:00	**Dinner**	

To Be Continued

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May 11, 2024 | Saturday

09:00-10:10	**Opening Ceremony**	Ru Huang, President of Southeast University, Academician of the Chinese Academy of Sciences						
		Yue Hao, Professor of Xidian University, Academician of the Chinese Academy of Sciences						
		Hui Chen, Deputy Secretary of the Party Working Committee of Xi'an Hi-tech Zone and Director of the Administrative Committee of Xi'an Hi-tech Zone						
		2023 EDA Contest Award Ceremony						
		Promotion for ISEDA 2025						
10:10-10:40	**Break**							
10:40-11:20	**Keynote Speech 1**	Jamal Deen: Compact Modeling of Organic/Polymeric Thin Film Transistors For Flexible Electronics						
11:20-12:00	**Keynote Speech 2**	David Atienza Alonso: Dynamic Thermal Management and Adaptive Modeling for 3D AI Chips						
12:00-13:30	**Lunch**		**Invited Speakers / Papers**					
13:30-15:30	**Technical Session 1**	Latest News From Lithography	184	159	19	27	163	105
	Technical Session 2	The Breakthrough in Testing	Sybille Hellebrand	Hans-Joachim Wunderlich	6	150	180	108
	Technical Session 3	Advanced Tactics in Design Methodology	Zebo Peng	179	106	92	45	
	Technical Session 4	Transient Simulation and Model Reduction	10	65	98	103	131	147
	Panel 1	2.5D/3D Heterogeneous Integration: Challenges and Opportunities						
	Forum	EDA Contest						
15:30-16:00	**Break**							
15:30-16:00	**Poster Session**		9	15	16	24	25	37
			60	66	86	94	95	100
			119	174	176	181	204	
16:00-18:00	**Technical Session 5**	Design Verification	Ying J Chen	40	3	212	137	
	Technical Session 6	The Open Source EDA Movement	Tsung-Yi Ho	Xingquan Li	31	129	160	57
	Technical Session 7	Leveraging Machine Learning in EDA	Peter Chun	Hui-Ling Zhen	182	188	20	96
	Technical Session 8	Multi-Physics Analysis and Simulation	Xiaohua Ma	Huanhuan Zhang	Xiaoyan Liu	Wenchao Chen	196	
	Technical Session 9	New Frontiers in Analog EDA	Xuan Zeng	172	185	51	152	168
	Forum	EDA Contest						
18:00	**Dinner**							

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May 12, 2024 | Sunday

09:00-09:40	**Keynote Speech 3**	Xiaoqing Wen: Power-Aware LSI Testing: Present and Future						
09:40-10:20	**Keynote Speech 4**	John Kim: The Hidden Interconnect (or Communication) Challenges						
10:20-10:50	**Break**							
10:50-11:30	**Keynote Speech 5**	Sreejit Chakravarty: EDA Challenges in Chiplet Interconnect Test and Repair						
11:30-12:10	**Keynote Speech 6**	Christopher Thomas: Trends in The Industry (Tentative)						
12:10-13:30	**Lunch**		**Invited Speakers / Papers**					
13:30-15:30	**Technical Session 10**	Advanced in EMIR and Parasitic Extraction	Wenjian Yu	115	97	109	194	
	Technical Session 11	Co-Optimizing Systems, Design, and Technology	Gordon Shou	34	Hrachya Astsatryan	127	21	
	Technical Session 12	Pushing the Envelope in Physical Implementation	30	18	35	87	124	
	Technical Session 13	Design, Safety and Reliability	169	68	78	102	183	
	Technical Session 14	Synthesis Techniques: The Next Generation	Yun Shao	213	114	85	132	
	Technical Session 15	Chiplet and 3DIC Revolution & High-Level Synthesis Frontier	Pei-Hsin Ho	83	74	63	205	
15:30-16:00	**Break**							
16:00-18:00	**Technical Session 16**	Memory Testing and Yield Enhancement	Xin Li	165	193	162	128	111
	Technical Session 17	EDA Strategies for FPGA Deployment	Hailong You	Jing Zhou	118	123	208	140
	Technical Session 18	Emerging Horizons in TCAD	Karen Gambaryan	8	36	107	177	91
	Panel 2	LLM for Chip Design: Challenge and Opportunities						
	Panel 3	The Future of Analog CAD: Navigating the Spectrum between Full Automation and Human Expertise						
	Panel 4	When Math Meets EDA: A Tale of Two Disciplines						
18:30	**Banquet**							

To Be Continued

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May 13, 2024 | Monday

09:00-09:40	**Keynote Speech 7**	Elyse Rosenbaum: Circuit Simulation of Integrated Circuit Response to ESD (Online)						
09:40-10:20	**Keynote Speech 8**	Jacky Ni: Manufacturing EDA in the Era of Generative AI						
10:20-10:40	**Break**							
10:40-11:20	**Keynote Speech 9**	Sa Zhao: Effective Yield Diagnosis – Bridging Design & Manufacturing						
11:20-12:00	**Keynote Speech 10**	Han Yu: Recent Progress of AI Algorithms for EDA						
12:00-12:30	**Keynote Speech 11**	Mehdi B. Tahoori: Printed Computing: Design Automation and Computing based on Additive Printed Electronics (Online)						
12:30-13:30	**Lunch**		**Invited Speakers / Papers**					
13:30-15:30	**Technical Session 19**	The Future of Placement	47	70	136	50	145	
	Technical Session 20	Design Space Exploration	144	49	73	4	189	
	Technical Session 21	Innovative Pathways in Routing	149	61	69	13	141	
	Technical Session 22	Exploring EDA Applications in HPC and AI	Xinliang Wang	Xiaoming Liu	Yutao Ma	2	38	
	Technical Session 23	Revolutionizing Timing Analysis	77	113	134	158	195	
	Technical Session 24	Thermal Management at Chip Level	1	89	198	64	72	
15:30-16:00	**Break**							
16:00-18:00	**Technical Session 25**	Device Simulation and Optimization	202	23	93	101	155	166
	Technical Session 26	Need More Acceleration? Use FPGA!	Yaowei Zhang	133	59	190	173	191
	Technical Session 27	Analog Insights: New Waves on Simulation and Analysis	Nan Zhang	32	48	84	157	210
	Technical Session 28	Mastering Synthesis Optimization	Lei Chen	167	62	46	170	146
	Technical Session 29	Process Modeling and Simulation in Modern Era	Geng Bai	125	201	203	88	171
	Technical Session 30	Compact Modeling for Circuit Innovation	26	76	82	122	135	187
18:00	**Dinner**							